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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,215	02/25/2002	Christopher Bentley Dornan	550-316	2852

23117 7590 06/29/2005

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EXAMINER	
ROCHE, TRENTON J	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,215	DORNAN ET AL.	
	Examiner	Art Unit	
	Trenton J. Roche	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communications filed 22 March 2005.

2. Claims 1-39 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,937,193 to Evoy.

Per claim 1:

Evoy discloses:

- An apparatus for processing data under control of a set of program instructions that map upon interpretation to data processing operations to be performed ("a computer system to execute program code in a format having platform independent instructions on a processor in the computer system that executes program code in a format having native instructions" in col. 2 lines 39-43)
- a fixed mapping hardware interpreter operable to interpret a fixed mapping group of said set of program instructions, whereby a program instruction from said fixed mapping group

maps to a fixed sequence of one or more data processing operations ("A first, native mode...of the processor...whereby 32-bit native instructions are pulled from system memory and executed directly by the processor..." in col. 4 lines 54-57. As the instructions are native, they are fixed to the hardware processor and do not require reprogramming and translation.)

- a programmable mapping hardware interpreter operable to interpret a programmable mapping group of said program instructions, whereby a program instruction from said programmable mapping group maps to a sequence of one or more data processing operation that varies in dependence upon programming of said programmable mapping hardware interpreter ("a second, platform-independent (Java) mode...utilized to receive 8-bit Java bytecode and output corresponding 32-bit native instructions directly to processor for execution..." in col. 4 lines 57-62)

substantially as claimed.

Per claim 2:

The rejection of claim 1 is incorporated, and further, Evoy discloses a software execution unit operable to interpret at least a software interpreted group of program instructions as claimed ("interpret the unmapped bytecode via a software interpreter" in col. 5 lines 66-67)

Per claim 3:

The rejection of claim 2 is incorporated, and further, Evoy discloses one or a combination of a software interpreter and a just in time compiler as claimed (Note the rejection regarding claim 2)

Per claim 4:

The rejection of claim 1 is incorporated, and further, Evoy discloses a fixed set of sequences of one or more data processing operations to which program instructions from said programmable mapping group may be mapped as claimed ("Each platform-independent instruction is matched with an entry in object table 51 by using the bytecode for the instruction as the index to the table. Each entry therefore includes a 32-bit native instruction that corresponds to the platform-independent instruction..." in col. 5 lines 53-57)

Per claim 5:

The rejection of claim 1 is incorporated, and further, Evoy discloses a programmable translation table that translates program instructions within said programmable mapping group into a sequence of one or more data processing operations to be performed as claimed ("object table 51 is implemented as a volatile RAM...programming of the table is permitted..." in col. 6 lines 32-35)

Per claim 6:

The rejection of claim 5 is incorporated, and further, Evoy discloses specifying a sequence of one or more data processing operations to be performed as claimed (Note at least Table III and the corresponding sections of the disclosure)

Per claim 7:

The rejection of claim 6 is incorporated, and further, Evoy discloses said programmable translation table is a content addressable memory addressed via a program instruction value to specify a

corresponding operation value (Note at least Table III and the corresponding sections of the disclosure)

Per claim 8:

The rejection of claim 6 is incorporated, and further, Evoy discloses a random access memory with a program instruction value being decoded to address a storage location within said random access memory for a corresponding operation value as claimed ("object table 51 is implemented as a volatile RAM..." in col. 6 lines 32-33)

Per claim 9:

The rejection of claim 5 is incorporated, and further, Evoy discloses an invalid entry trap operable to block storage of unsupported mappings within said translation table ("This bit is set whenever no native instruction exists that can be directly mapped to the addressing bytecode..." in col. 5 lines 59-61)

Per claim 10:

The rejection of claim 1 is incorporated, and further, Evoy discloses processing operations equivalent to one or more native program instructions of a processor core that is a target for said fixed mapping hardware interpreter and said programmable mapping hardware interpreter as claimed ("each entry therefore includes a 32-bit native instruction that corresponds to the platform-independent instruction..." in col. 5 lines 55-57)

Per claim 11:

The rejection of claim 1 is incorporated, and further, Evoy discloses Java bytecodes as claimed ("Java bytecodes..." in col. 4 line 21)

Per claim 12:

The rejection of claim 2 is incorporated, and further, Evoy discloses a software interpreted group including all those instructions not within said fixed mapping group or said programmable mapping group as claimed ("a 33rd bit is also included...this bit is set whenever no native instruction exists that can be directly mapped...the exception signal is provided as a data signal...to allow the processor to return to native mode and interpret the unmapped bytecode via a software interpreter..." in col. 5 lines 58-67)

Per claim 13:

The rejection of claim 12 is incorporated, and further, Evoy discloses a software interpreted group including all of said program instructions, said software interpreter being invoked when neither said fixed mapping hardware interpreter or said programmable mapping hardware interpreter can interpret a program instruction as claimed ("a 33rd bit is also included...this bit is set whenever no native instruction exists that can be directly mapped...the exception signal is provided as a data signal...to allow the processor to return to native mode and interpret the unmapped bytecode via a software interpreter..." in col. 5 lines 58-67)

Per claim 14:

The rejection of claim 1 is incorporated, and further, Evoy discloses said fixed mapping hardware interpreter and said programmable mapping hardware interpreter sharing at least some decoder hardware as claimed (Note Figure 2 and the corresponding sections of the disclosure)

Per claim 15:

The rejection of claim 1 is incorporated, and further, Evoy discloses a translation pipeline stage with a program instruction buffer operable to store program instructions to be interpreted providing an input to said translation pipeline stage such that program instructions are subject to a programmable mapping within said translation pipeline stage prior to further interpretation as claimed (Note Figure 2 and the corresponding sections of the disclosure)

Per claims 16-30:

Claims 16-30 recite method claims corresponding to the apparatus disclosed in claims 1-15, respectively, and are rejected for the reasons set forth in connection with claims 1-15, respectively.

Per claims 31, 32-34, 35, 36, 37, 38 and 39:

Claims 31, 32-34, 35, 36, 37, 38 and 39 recite computer program product claims corresponding to the apparatus disclosed in claims 1, 4-6, 9, 10, 11, 2 and 3, respectively, and are rejected for the reasons set forth in connection with claims 1, 4-6, 9, 10, 11, 2 and 3, respectively.

Response to Arguments

5. Applicant's arguments, see pages 11-13 of the remarks, filed 22 March 2005, with respect to the rejection(s)of claim(s) 1-39 have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of alternate prior art of record.

Per claims 1, 16 and 31:

As noted above, the Examiner interpreted the first mapping hardware interpreter recited in claim 1 to correspond to the execution of straight native code, as the native code has a fixed mapping in the processor and does not require a programmed translation. The programmable mapping hardware interpreter is therefore interpreted to correspond to the method of mapping platform-independent instructions to native instructions via a programmable object table as disclosed by Evoy.

However, for the sake of argument, the limitations of independent claims 1, 16 and 31 could be interpreted in an alternate way; mainly, that since the object table of Evoy provides a direct mapping, the translation of platform-independent instructions to native instructions via the object table represents the fixed mapping hardware interpreter, since the mappings are direct. Furthermore, the programmable mapping hardware interpreter would correspond to the native processor which is executing a software interpreter. Since the software interpreter, which provides programmable mapping, is utilized to map bytecodes to a specific native instruction that is recognizable by the processor, then the processor and interpreter can be reasonably interpreted as being a programmable mapping hardware interpreter.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trenton J. Roche whose telephone number is (571) 272-3733. The examiner can normally be reached on Monday - Friday, 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trenton J Roche
Examiner
Art Unit 2193

TJR

ANIL KHATRI
PRIMARY EXAMINER